

(A High Impact Factor, Monthly, Peer Reviewed Journal) Visit: <u>www.ijirset.com</u>

Vol. 8, Issue 5, May 2019

Removing Baseline Wandernoise Using Infinite Impulse Response IIR Low Pass Filter

M.Dhivyaa^{#1}, V.Gopalakrishnan^{*2}

Associate Professor, Department of ECE, Sasurie College of Engineering, Vijayamangalam, Tirupur,

Tamilnadu, India^{#1}

II-M.E-VLSI Design, Department of ECE, Sasurie College of Engineering, Vijayamangalam, Tirupur,

Tamilnadu, India^{*2}

ABSTRACT: The proposed design for analyzing electrocardiography (ECG) signals. This methodology employs low pass least-square linear phase infinite impulse response (IIR) filtering technique to filter out the baseline wander noise embedded in the input ECG signal to the system. Discrete wavelet transform (DWT) was utilized as a feature extraction methodology to extract the reduced feature set from the input ECG signal. The design uses back propagation neural network classifier to classify the input ECG signal. The system is simulation on MATLAB and Xilinx system generator.

I. INTRODUCTION

In recent years, cardiovascular disease, including heart disease and stroke, remains the leading cause of death around the world. Yet most heart attacks and strokes could be prevented if some method of pre-monitoring and pre-diagnosing can be provided. In particular, early detection of abnormalities in the function of the heart can be valuable for clinicians. Studying the electrocardiogram (ECG) signal provides an insight to understand life-threatening cardiac conditions.

This typically is centered on the study of arrhythmias, which can be any disturbance in the rate, regularity, and site of origin or conduction of the cardiac electric impulse. Not all arrhythmias are abnormal or dangerous but some do require immediate therapy to prevent further problems. A subject's ECG information can be recorded using a portable Holter monitor which is worn by the subject. A Holter monitor typically employs a few electrodes and stores a recording of the subject's heart rhythm as they go about their daily activities over a 24–48 h period.

The Holter monitor is then returned to a cardiologist who examines the recordings and determines a diagnosis. Examining these recordings is a time-consuming and hence any automated processing of the ECG that assists the cardiologist in determining a diagnosis would be of assistance. The basic problem of automating ECG analysis occurs from the non-linearity in ECG signals and the large variation in ECG morphologies of different patients. And in most cases, ECG signals are contaminated by background noises, such as electrode motion artifact and electromyogram-induced noise, which also add to the difficulty of automatic ECG pattern recognition.

Many researches depend on digital signal processing (DSP) techniques as a methodology to design automated ECG signal analysis systems. Most DSP systems use typical main stages for analyzing ECG signals; those main stages include denoising stages, feature extraction stages, and classification stages. This work discusses the problem of analyzing of electrocardiography (ECG) signals. A new system for analyzing ECG is presented. This system uses least-square linear phase FIR filter(LLFE) methodology to overcome the limitations of the previous methodologies.

II. LITERATURE SURVEY

According to recent physiological experiments, the envelope and phase of speech signals are required to enhance the perceptive capability of a cochlear implant processor. In this paper, the design of an analog complex gamma tone filter



(A High Impact Factor, Monthly, Peer Reviewed Journal)

Visit: www.ijirset.com

Vol. 8, Issue 5, May 2019

is introduced in order to extract both envelope and phase information of the incoming speech signals as well as to emulate the basilar membrane spectral selectivity. The gamma tone impulse response is first transformed into the frequency domain and the resulting 8th-order transfer function is subsequently mapped onto a state-space description of an orthonormal ladder filter. Using this approach, the real and imaginary transfer functions that share the same denominator can be extracted using two different C matrices. This results in a compact filter structure.

This paper examines a number of stochastic computational elements employed in artificial neural networks, several of which are introduced for the first time, together with an analysis of their operation. We briefly include multiplication, squaring, addition, subtraction, and division circuits in both unipolar and bipolar formats, the principles of which are well-known, at least for unipolar signals. We have introduced several modifications to improve the speed of the division operation. The primary contribution of this paper, however, is in introducing several state machine-based computational elements for performing sigmoid nonlinearity mappings, linear gain, and exponentiation functions. We also describe an efficient method for the generation of, and conversion between, stochastic and deterministic binary signals. The validity of the present approach is demonstrated in a companion paper through a sample application, the recognition of noisy optical characters using soft competitive learning. Network generalization capabilities of the stochastic network maintain a squared error within 10 percent of that of a floating-point implementation for a wide range of noise levels. While the accuracy of stochastic computation may not compare favorably with more conventional binary radix-based computation, the low circuit area, power, and speed characteristics may, in certain situations, make them attractive for VLSI implementation of artificial neural networks.

This paper introduces a design of a gammatone filter based on stochastic computation for area-efficient hardware. The gammatone filter well expresses the performance of human auditory peripheral mechanism and has a potential of improving advanced speech communications systems, especially hearing assisting devices and noise robust speech recognition systems. Using stochastic computation, a power-and-area hungry multiplier used in a digital filter is replaced by a simple logic gate, leading to area-efficient hardware. However, a straightforward implementation of the stochastic gammatone filter suffers from significantly low accuracy in computation, which results in a low dynamic range (a ratio of the maximum to minimum magnitude) due to a small value of a filter gain. To improve the computational accuracy, gain-balancing techniques are presented that represent the original gain as the product of multiple larger gains introduced at the second-order sections. As a result, the proposed techniques maintain the original gain of the filter while improving the computational accuracy. The proposed stochastic gammatone filters are designed and evaluated using MATLAB that achieves a high dynamic range of 71.71 dB compared with a low dynamic range of 5.47 dB in the straightforward implementation.

Stochastic decoding is a new approach to iterative decoding on graphs. This paper presents hardware architecture for fully parallel stochastic low-density parity-check (LDPC) decoders. To obtain the characteristics of the proposed architecture, we apply this architecture to decode an irregular state-of-the-art (1056,528) LDPC code on a Xilinx Virtex-4 LX200 field-programmable gate-array (FPGA) device.

Nowadays, there are many commercial ANC (Active Noise Control) headphones using either digital signal processors (DSPs) as control unit to implement the feedback FXLMS algorithm, or analog circuit by using control theory's feedback structure to cancel the noise in active way. However, for DSP's product, it's much expensive than conventional passive headphone. As a result, this paper proposed using a micro-controller unit (MCU), Cortex-M4, instead of DSP to implement the adaptive algorithm in headsets. Experimental results illustrate the digital control ANC headsets' performance with commercial headset to verify effectiveness.

III. METHODS

FIR-filters:

In signal processing, a causal filter is a linear and time-invariant causal system. The word causal indicates that the filter output depends only on past and present inputs. A filterwhose output also depends on future inputs is non-causal, whereas a filter whose output depends only on future inputs is anti-causal. Systems (including filters) that are realizable (i.e. that operate in real time) must be causal because such systems cannot act on a future input. In effect that means the output sample that best represents the input at time comes out slightly later. A common design practice for digital



(A High Impact Factor, Monthly, Peer Reviewed Journal)

Visit: www.ijirset.com

Vol. 8, Issue 5, May 2019

filters is to create a realizable filter by shortening and/or time-shifting a non-causal impulse response. If shortening is necessary, it is often accomplished as the product of the impulse-response with a window function.



Fig 1:Causal FIR Filters diagram

ELLIPTIC FILTER

These type of the filters are flexible than the FIR filter because of their feedback from previous output. As compared to FIR, denominator provides freedom in shape and response of the filter. Therefore design of IIR filter is simpler. These filters works on the approximations like Butterworth, Chebyshev and Elliptic. The Elliptic approximation has equiripple response in both passband and stopband. The frequency response magnitude of the elliptic filter of the order N is given by



Fig.2.a: Magnitude Response



(A High Impact Factor, Monthly, Peer Reviewed Journal)

Visit: <u>www.ijirset.com</u>

Vol. 8, Issue 5, May 2019



Fig.2. b: Phase Delay Response

Also known as Cauer filters, Elliptic filters are equiripple in both the passband and stopband. They generally meet filter requirements with the lowest order of any supported filter type. For a given filter order, passband ripple, and stopband ripple, elliptic filters minimize transition width.

IIR Filtering

Digital filters play a crucial role in digital signal processing, e.g., biomedical signal processing. A digital filter refers to a mathematical algorithm executed in hardware/software which works on a digital input signal to generate a digital output signal so as to achieve a filtering objective. The term digital filter employed in this paper refers to the software filter.

Digital IIR filters could be designed to be low pass, high pass, band pass or band stop. One can modify band stop filter to work as a notch filter. Digital IIR filters are developed from its analog counterpart using different methods like impulse invariant, bilinear z-transform or matched z-transform. Some of the important analog counterparts of digital IIR filters include butterworth low pass, butterworth high pass, chebyshev low pass and chebyshev high pass.



Fig. 3: Block diagram of IIR filter

In a design problem in which no ripple is acceptable in pass band and stop band, Butterworth filter can be a better choice. But due to no-linear phase response, the waveform becomes distorted. The Magnitude Response and Phase Response of Butterworth low pass filter is shown in figures



(A High Impact Factor, Monthly, Peer Reviewed Journal) Visit: <u>www.ijirset.com</u> Vol. 8, Issue 5, May 2019

IV. RESULTS AND DISCUSSION

4.1. SIMULATION RESULTS OF EXISTING DIVIDER



Fig: 4. SIMULATION RESULTS OF PROPOSED



Fig: 5. Input signal:



(A High Impact Factor, Monthly, Peer Reviewed Journal)

Visit: <u>www.ijirset.com</u> Vol. 8, Issue 5, May 2019





V. CONCLUSION

The proposed design is used for analyzing electrocardiography (ECG) signals. This methodology employs low pass least-square linear phase infinite impulse response (IIR) filtering technique to filter out the baseline wander noise embedded in the input ECG signal to the system. Discrete wavelet transform (DWT) is utilized as a feature extraction methodology to extract the reduced feature set from the input ECG signal. The design uses back propagation neural network classifier to classify the input ECG signal and give accurate measurement of the heart signal.

REFERENCES

[1] M. Alioto, "Ultra-low power VLSI circuit design demystified and explained: A tutorial," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 59, no. 1, pp. 3–29, Jan. 2012.

[2] V. Gupta, D. Mohapatra, A. Raghunathan, and K. Roy, "Low-power digital signal processing using approximate adders," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 32, no. 1, pp. 124–137, Jan. 2013.

[3] H. R. Mahdiani, A. Ahmadi, S. M. Fakhraie, and C. Lucas, "Bio-inspired imprecise computational blocks for efficient VLSI implementation of soft-computing applications," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 4, pp. 850–862, Apr. 2010.

[4] R. Venkatesan, A. Agarwal, K. Roy, and A. Raghunathan, "MACACO: Modeling and analysis of circuits for approximate computing," in Proc. Int. Conf. Comput.-Aided Design, Nov. 2011, pp. 667–673.

[5] F. Farshchi, M. S. Abrishami, and S. M. Fakhraie, "New approximate multiplier for low power digital signal processing," in Proc. 17th Int. Symp. Comput. Archit. Digit. Syst. (CADS), Oct. 2013, pp. 25–30.

[6]Vladimir M. Poučki, Andrej Žemva, Miroslav D. Lutovac "Elliptic IIR filter sharpening implemented on FPGA" Digital signal processing Vol. 20, Issue 1, January 2010, pp13–22.

[7]Chavan M S, Agarwala R A, and Uplane M D, Supperssion of Baseline Wandeand PowerlineINterference in ECG Using Digital IIR Filter .(2008)

[8]RanjeetaVerma, Pooja Singh and Rajesh Mehra, "Resource Estimation for Design of IIR Filters using Polyphase Decomposition", International Conference on Emerging Trends in Engineering and Technology, Vol. 3, no. pp. 26-31, 2013

[9] Sunil Kumar Yadav, Rajesh Mehra "Analysis of Different IIR Filter Based on Implementation Cost Performance" International Journal of Engineering and Advance Technology, Vol. 3, no. 4, pp. 267-270, April 2014

[10] Bashar A. Rajoub, An Efficient Coding Algorithm for the Compression of ECG Signals Using the Wavelet Transform, IEEE Transactions on Biomedical Engineering, Vol. 49, No. 4, April 2002.

[11] Chandak, P.R., Giradkar, V.P & Wadmalwar, A.T., (February 2015) "Design of FIR filter using Matlab Simulink and Xilinx system Generator" International Journal Of Engineering And Computer Science ISSN:2319-7242 Volume 4 Issue 2 Page No. 10384-10387.